REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-51 are presently active; Claim 48 has been presently amended. No new matter has been added.

In the outstanding Office Action, Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,583. Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,138. Claims 1-51 were rejected under 35 U.S.C. § 112, first paragraph, as based on non-enabling disclosure. Claim 48 was rejected under 35 U.S.C. § 101 for being non-statutory. Claims 1-51 were rejected under 35 U.S.C. § 102(e) as being unpatentable over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Jain et al (Mathematical Physical Engine ...).

Regarding the rejection on the merits:

Briefly recapitulating, Claim 1 defines a method of facilitating a process performed by a semiconductor processing tool including:

> 1) inputting process data relating to an actual process being performed by the semiconductor processing tool,
> 2) inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool,
> 3) performing first principles simulation ***for the actual process being performed*** using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, and
> 4) using the simulation result as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.[1]

[1] The enumerations have been added purely for the purpose of referencing these elements in the present

The claim defines clearly a process where data input from an actual process being performed is used for producing a first principles simulation result, produced for the actual process being performed during performance of the actual process. The result obtained is then used as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.

The Office Action states on pages 4 and 5 that:[2]

> Applicant alleges that, "Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process and not the claimed performing first principles simulation for the actual process being performed during performance of the actual process."
>
> The deficiency in the argument relates to Sonderman *teaching away* from performing concurrent simulation and actual processing. As asserted earlier, there is no such disclosure in Sonderman, and all the facts point towards, contrary to applicant's assertion of teaching away, that the simulation can be performed with actual process (Sonderman: Fig. 1-3) and sequentially with feedback to the actual process for the subsequent processes/wafers (Sonderman: Col. 9 Lines 45-61).

Applicant respectfully disagrees with the examiner's asserted position that "all facts point to the contrary." From the Sonderman et al disclosure, Applicant respectfully points out that, at col. 9, lines 46-51, Sonderman et al specifically discloses:

> The system 100 then optimizes the simulation (described above) ***to find more optimal process target*** (T_i) for each silicon wafer, S_i ***to be processed***. These target values are then used ***to generate new control inputs***, X_{Ti}, on the line 805 to control ***a subsequent process*** of a silicon wafer S_i. The ***new control inputs***, X_{Ti}, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like. [Emphasis added]

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discussion.

[2] The underscored limitation from the outstanding Office Action reproduced here is from one of the related applications and should have referred to the last step in Claim 1 of using the virtual sensor measurement obtained during the performance of the actual process to facilitate the actual process being performed by the semiconductor processing tool.

Thus, this section of Sonderman et al clearly discloses that the simulation is to find a more optimum process target for each silicon wafer ***to be processed***. The simulation results produce a new control input for the silicon wafer ***to be processed***. Thus, Applicant respectfully submits that Sonderman et al teach performing first principles simulation for the actual process to be performed ***before*** performance of the actual process, and **not** the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.

Other sections of Sonderman et al. support Applicant's position on this matter.

For instance, reproduced below is Figure 4 of Sonderman et al which clearly shows that the simulation results are produced ***ahead of performing a process*** and thus have to be based on historical data, and not based on the actual process being performed during performance of the actual process.

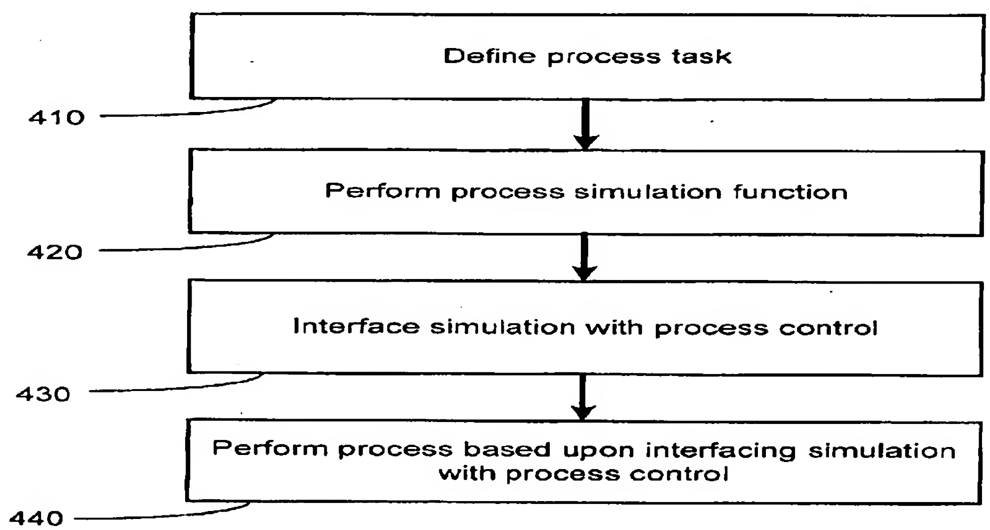

FIGURE 4

With reference to Figure 4, Sonderman et al disclose at col. 6, lines 24-47:

Turning now to FIG. 4, a flow chart representation of the methods in accordance with the present invention is illustrated. In one embodiment, ***the system 100 defines a process task that is to be performed (block 410).*** The process task maybe a photolithography process, an etching process, and the like. ***The system 100 then performs a process simulation function*** (block 420). A more detailed description of the process simulation function described in block 420, is illustrated below. In one embodiment, a simulation data set results from the execution of the process simulation function.

Once the system 100 performs the process simulation function, the system 100 performs an interfacing function, which facilitates interfacing of the simulation data with the process control environment 180 (block 430). The process control environment 180 can utilize the simulation data in order to modify or define manufacturing control parameters that control the actual processing steps performed by the system 100. ***Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 then performs a manufacturing process*** based upon the manufacturing parameters defined by the process control environment 180 (block 440). [Emphasis added]

Hence, the process flow in Sonderman et al is straightforward:

1) define process to be modeled,

2) model process for simulation result,

3) interface simulation result to processor, and then

4) run the process under control based on the pre-existing simulation result.

Note also that this sequence in Sonderman et al means that Sonderman et al do not disclose inputting process data relating to an actual process being performed by the semiconductor processing tool, as also claimed. Rather, Sonderman et al use data from previous runs to produce a simulation result.

Accordingly, Applicant respectfully submits that Sonderman et al do not disclose and indeed ***teach away*** from the present invention.

Furthermore, the deficiencies in Sonderman et al are not overcome by Jain et al. In the present case, the Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Jain et al.

Jain et al disclose at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations. Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

Moreover, the proposed development work in Jain is understood better in the light of the "conventional approach" referred to by Kee et al, made of record by the Information Disclosure Statement filed December 20, 2005.

For instance, Kee et al in detail disclose that:

> The modeling apparatus 101 of the instant invention may also be used to perform an inverse analysis to establish the boundary conditions or parameter values required to achieve a certain function of the thermal system. This allows the apparatus to be used to establish the appropriate process parameters and boundary conditions for the thermal system modeled. In accordance with the instant invention, the inverse analysis can be directly carried out by the modeling apparatus ***rather than using the conventional approach, which merely solves the direct problem repeatedly, in a lengthy and costly iterative process***, to determine appropriate input parameters to achieve a desired result. In other words, in accordance with the instant invention, ***once a particular thermal process is modeled for a particular set of control parameters***, the device may then be used to automatically obtain

> the necessary control parameters to achieve a desired result by providing the modeling apparatus with parameters corresponding to the desired result.
>
> To carry out the inverse analysis, the modeling apparatus 101 includes an inverse parameter input section 104 also connected to input device 103. A user inputs into the modeling apparatus 101 parameters corresponding to desired results, e.g., desired temperature characteristics of the system, which are stored in memory 108. The processing unit 110, under control of modeling program 111, ***uses the previously generated model*** of the thermal system and the parameters held in memory 108 and derives or predicts particular control parameters to meet the constraints entered through the inverse parameter input section 104. This process is more fully described below in connection with the examples provided.[3] [emphasis added]

Hence, Kee et al explicitly disclose that the ***predicted*** model of the thermal system is used to design and control the thermal system. Kee et al exemplify the difficulties of a "conventional approach" which merely solves the spectral radiation transport equations through "a lengthy and costly process." These problems forced Kee et al to use ***pre-generated model results*** for a control process.

M.P.E.P. § 2143.01(II) states that

> The test for obviousness is what the ***combined teachings of the references*** would have suggested to one of ordinary skill in the art, and ***all teachings in the prior art must be considered*** to the extent that they are in analogous arts. When the teachings of two or more prior art references conflict, the Examiner ***must weigh the power of each reference to suggest solutions*** to one of ordinary skill in the art, considering the degree to which one reference ***might accurately discredit another***. [Emphasis added.]

It appears that the Examiner has not considered the degree to which Jain et al and Kee et al discredit any suggestion that the examiner may have read from the disclosure of Sonderman et al.

The Supreme Court in *KSR International Co. v. Teleflex Inc. et al. 2007 U.S. LEXIS 4745* reinforced the role of *Graham* factors and "teaching away" in deciding obviousness. The Court stated that:

> In *United States v. Adams*, 383 U. S. 39, 40 (1966), a companion case to *Graham*, the Court considered the obviousness of a wet battery that varied

[3] Kee et al, col. 4, lines 21-50.

> from prior designs in two ways: It contained water, rather than the acids conventionally employed in storage batteries; and its electrodes were magnesium and cuprous chloride, rather than zinc and silver chloride. The Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result. 383 U. S., at 50-51. It nevertheless rejected the Government's claim that Adams's battery was obvious. The Court relied upon the corollary principle that when the prior art ***teaches away*** from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.*, at 51-52. When Adams designed his battery, the prior art warned that risks were involved in using the types of electrodes he employed. The fact that the elements worked together in ***an unexpected and fruitful manner*** supported the conclusion that Adams's design was ***not obvious*** to those skilled in the art. [Emphasis added.]

In the present situation, the claimed method of performing a first principles simulation ***for the actual process being performed during performance of the actual process*** produces ***more than an expected result*** in that Sonderman et al (in having to develop a ***new control inputs*** for each subsequent wafer) can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process. Indeed, as pointed out above, the examiner considered it an impossibility to simultaneously perform a first principles simulation result and to control the actual process being run with the first principles simulation result. Hence, the claimed processes and systems produce ***an unexpected result.***

Viewed differently, Applicants' position on this matter is consistent with a number of the *Graham* factors identified in M.P.E.P. § 2141 III as objective evidence of non-obviousness.

The failure of both Sonderman et al and Jain et al to produce themselves the claimed invention due to the real and technical problems encountered represents ***a failure of others*** to produce the claimed invention. Moreover, the achieving of a system which can perform a

first principles simulation for the actual process being performed during performance of the actual process provides ***an unexpected result***, as compared to the prior art capability.

For all these reasons, Applicant submits that the present invention patentably defines over Sonderman et al and Jain et al.

Regarding the rejection under 35 U.S.C. § 112, first paragraph:

M.P.E.P. § 2164.01 states that the test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. Applicant submits that the exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct the first principle simulation model is disclosed by Applicant's specification by numbered paragraphs [0035] and [0036] which state that

> First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used.
>
> First principles simulation processor 108 is a processing device that applies data input from the data input device 104 to the first principles physical model 108 to execute a first principles simulation. Specifically, the first principles

> simulation processor 108 may use the data provided by the data input device 104 to set initial conditions and/or boundary conditions for the first principles physical model 106, which is then executed by the simulation module. First principles simulations in the present invention include, but are not limited to, simulations of electro-magnetic fields derived from Maxwell's equations, continuum simulations, for example, for mass, momentum, and energy transport derived from continuity, the Navier-Stokes equation and the First Law of Thermodynamics, as well as atomistic simulations derived from the Boltzmann equation, such as for example Monte Carlo simulations of rarefied gases (see Bird, G.A. 1994. Molecular gas dynamics and the direct simulation of gas flows, Clarendon Press). First principles simulation processor 108 may be implemented as a processor or workstation physically integrated with the semiconductor processing tool 102, or as a general purpose computer system such as the computer system 1401 of Figure 14. The output of the first principles simulation processor 108 is a simulation result that is used to facilitate a process performed by the semiconductor processing tool 102. For example, the simulation result may be used to facilitate process development, process control and fault detection as well as to provide virtual sensor outputs that facilitate tool processes, as will be further described below.

Furthermore, Claims 7, 9 and 10 as further supported in the specification provide details of inputting data and computer codes for performing the first principles simulation result.

Thus, one of ordinary skill in the art, knowing from the specification that these codes are commercially available software programs, would not have to use undue experimentation to apply the respective physical attributes that each model is tailored to in order to perform the claimed inputting a first principles physical model step.

Hence, it is respectfully submitted that the 35 U.S.C. § 112, first paragraph, rejection should be withdrawn.

Regarding the rejection under 35 U.S.C. § 101:

Claim 48 has been amended as suggested in the outstanding Office Action. Thus, it is respectfully requested that the rejection to Claim 48 under 35 U.S.C. § 101 has been overcome.

Regarding the provisional double-patenting rejection:

Applicants submit that a terminal disclaimer can be filed, if the claims in the present application and the claims in the co-pending Application No. 10/673,507 remain obvious in view of each other at the time of allowance of either of these applications. Indeed, M.P.E.P. § 804.02 IV states that, prior to issuance, it is necessary to disclaim each one of the double patenting references applied. Hence, Applicants respectfully request that the examiner contact the undersigned should the present arguments be accepted and should the case be otherwise in a condition for allowance. At that time, a terminal disclaimer can be supplied to expedite issuance of this case.

Conclusion:

As argued above, the outstanding rejections for this patent application should be removed, placing all the claims in a condition for allowance.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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